UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,098	04/10/2006	Tsuyoshi Matsushita	071971-0566	3649

20277 7590 08/13/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
08/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,098	MATSUSHITA, TSUYOSHI	
	Examiner	Art Unit	
	LONG NGUYEN	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/10/06 + 1/7/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Specie I (Figures 1-3) in the reply filed on 5/4/09 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant indicates that claims 1-3, 7 and 8 are readable on the elected specie I (Figures 1-3).

Claim Objections

2. Claims 1-3, 7 and 8 are objected to because of the following informalities:

In claim 1-3, "resistance" should be changed to --resistance element-- since resistance, by itself, is not a physical element.

Claims 7 and 8 are objected to because they include the informality of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For claim 7, the recitation "wherein the drains of the first and second N-channel transistors serve as differential output terminals" is indefinite because it is not clear if the differential output terminals are in addition to the "output terminal" recited in earlier in claim 1,

or whether is output terminal recited in claim 1 is one of the differential output terminals. To overcome this problem, it is suggested that the recitation "an output terminal" in claim 1 be changed to --a first output terminal--, and the recitation "wherein the drains of the first and second N-channel transistors serve as differential output terminals" in claim 7 be changed to --wherein the drain of the first N-channel transistors serves as a second output terminal, wherein the first and second output terminals are differential output terminals--. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimazaki et al. (US 2001/0043085 A1).

With respect to claims 1 and 8, Figure 12 of Shimazaki et al. teaches a level shift circuit (20), which includes: first (MP11) and second (MP10) P-channel transistors; a high voltage power supply (VDDH); first (MN15) and second (MN14) N-channel transistors; complement input signals (D and D/ which is the output of INV); wherein a drain of the first N-channel transistor (MN15) is connected to a drain of the first P-channel transistor (MP11) and a gate of the second P-channel transistor (MP10) (by way of MN11), a drain of the second N-channel transistor (MN14) is connected to a drain of the second P-channel transistor (MP10) and a gate of the first P-channel transistor (MP11) (by way of MN10); the level shift circuit (10) further

comprises a resistance element (MN17) connecting the drain of the first N-channel transistor (MN15) with the drain of the second N-channel transistor (MN14), and wherein the drain of the second N-channel transistor (MN14) servers as an output terminal to a high power supply voltage operating circuit (transistor MN10 turns on which connected the drain of MN14 to node N2 and thus provides an output of the level shift circuit).

For claim 3, Figure 12 shows the resistance element (MN17) is constructed of an N-channel transistor (MN17) having its gate connected to a high-voltage power supply (VDDH).

For claim 7, Figure 12 shows the drains of the first and second N-channel transistors serve as differential output terminals for the high power-supply voltage operating circuit (by way of MN11 and MN10 as similar discussion in claim 1).

7. Claims 1 and 8 are also rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (USP 6,489,828).

With respect to claims 1 and 8, Figure 3 of Wang et al. teaches a level shift circuit, which includes: first (MP2) and second (MP3) P-channel transistors; a high voltage power supply (VDDH); first (MN2) and second (MN3) N-channel transistors; complement input signals (216 and 217) and a resistance element (MN4) connected as recited in claim 1 and wherein the drain of the second N-channel transistor (MN3) servers as an output terminal (OUT) to a high power supply voltage operating circuit.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimazaki et al. (US 2001/0043085 A1) in view of Shin et al. (USP 5,378,932).

With respect to claim 2, Figure 12 of Shimazaki et al. teaches a level shift circuit (20) which includes all the limitations of this claim except for the resistance element comprising a P-channel transistor having its gate connected to ground so as the P-channel transistor of the resistance means is normally ON. However, Shin et al. teaches in Figure 13 a resistance element that is constructed of a PMOS transistor having its gate connected to ground so as the PMOS transistor is normally ON. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the level shift circuit (20) in Figure 12 of Shimazaki et al. by using the resistance means that is constructed of a P-channel transistor having its gate connected to ground as taught in Figure 13 of Shin et al. since the circuitry would have been functionally equivalent and that the circuit designer would have more flexibility in designing the circuitry depending on the availability of the materials when designing the circuitry. Thus, this medication/combination meets all the limitations of claim 2.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Long Nguyen/
Primary Examiner
Art Unit 2816